What is claimed is:

1. A nonvolatile ferroelectric memory device, comprising:

a memory control block for outputting control signals in response to a write enable command signal, a read enable command signal and a reset signal, wherein the control signals control data read/write operations;

a ferroelectric memory cell array for writing the data, and reading data stored in a sense amplifier in response to the control signals; and

a power-up reset circuit for outputting the reset signal to restore data stored in the ferroelectric memory cell array.

2. The nonvolatile ferroelectric memory device of claim 1, wherein the ferroelectric memory cell array comprises:

a plurality of bitline pairs;

a plurality of first single port memory cells connected in column direction between a pair of the bitlines; and

the sense amplifier connected between one of the plurality of bitline pairs.

3. The nonvolatile ferroelectric memory device of

claim 2, wherein the first single port memory cell comprises:

a first latch means for amplifying a high level by using the voltage difference among output nodes;

a write control means for selectively connecting the bitlines to output nodes in response to the control signal;

a storage means including a plurality of ferroelectric capacitors;

a second latch means for amplifying a low level by using the voltage difference among output nodes;

a pull-up switch for selectively applying a power supply voltage to the first latch means in response to the control signal; and

a pull-down switch for selectively connecting the second latch means to a ground voltage in response to the control signal.

4. The nonvolatile ferroelectric memory device of claim 3, wherein the first latch means comprises cross-coupled PMOS transistors between the output nodes.

5. The nonvolatile ferroelectric memory device of claim 3, wherein the storage means comprises:

first and second ferroelectric capacitors having one terminal connected to the output nodes respectively and

the other terminal commonly receiving the control signal; and

third and fourth ferroelectric capacitors having one terminal connected to the output nodes respectively and the other terminal connected to a ground voltage.

6. The nonvolatile ferroelectric memory device of claim 5, wherein the number of the third and fourth ferroelectric capacitors increases according to the loading level of the output nodes.

7. The nonvolatile ferroelectric memory device of claim 1, wherein the ferroelectric memory cell array comprises:

a plurality of bitline pairs;

a plurality of common pull-up lines;

a plurality of common pull-down lines;

a plurality of pull-up means for selectively applying a power supply voltage to the plurality of common pull-up lines respectively in response to the control signal;

a plurality of pull-down means for selectively connecting the plurality of common pull-down lines with ground voltages respectively in response to the control signal;

a plurality of second single port memory cells

connected in column direction between a pair of the bitlines; and

the sense amplifier connected between one of the plurality of bitline pairs.

8. The nonvolatile ferroelectric memory device of claim 7, wherein the second single port memory cell comprises:

a first latch means for amplifying a high level by using the voltage difference between output nodes;

a write control means for selectively connecting the bitlines to output nodes in response the control signal;

a storage means including a plurality of ferroelectric capacitors; and

a second latch means for amplifying a low level by using the voltage difference between output nodes.

9. The nonvolatile ferroelectric memory device of claim 8, wherein the first latch means comprises cross-coupled PMOS transistors between the output nodes.

10. The nonvolatile ferroelectric memory device of claim 8, wherein the storage means comprises:

first and second ferroelectric capacitors having one terminal connected to the output nodes respectively and

the other terminal commonly receiving the control signal; and

third and fourth ferroelectric capacitors having one terminal connected to the output nodes respectively and the other terminal connected to a ground voltage.

11. The nonvolatile ferroelectric memory device of claim 10, wherein the number of the third and fourth ferroelectric capacitors is increased according to the loading level control of the output nodes.

12. The nonvolatile ferroelectric memory device of claim 1, wherein the ferroelectric memory cell array comprises:

a plurality of write bitline pairs;

a plurality of read bitline pairs;

a plurality of first multi port memory cells connected in column direction between one of the plurality of write bitline pairs and one of the plurality of read bitline pairs;

a write driving means connected between one of the plurality of write bitline pairs; and

a sense amplifier connected between one of the plurality of read bitline pairs.

13. The nonvolatile ferroelectric memory device of

claim 12, wherein the first multi port memory cell comprises:

a first latch means for amplifying a high level by using the voltage difference between output nodes;

a plurality of write control means for selectively connecting the write bitline pairs to output nodes in response to the control signal;

a storage means including a plurality of ferroelectric capacitors;

a second latch means for amplifying a low level by using the voltage difference between output nodes;

a plurality of read control means for changing a voltage level of the read bitline pairs in response to the control signal and a potential of the output nodes;

a pull-up switch for selectively applying a power supply voltage to the first latch means in response to the control signal; and

a pull-down switch for selectively connecting the second latch means to a ground voltage in response to the control signal.

14. The nonvolatile ferroelectric memory device of claim 13, wherein the first latch means comprises cross-coupled PMOS transistors between the output nodes.

15. The nonvolatile ferroelectric memory device of

claim 13, wherein the storage means comprises:

first and second ferroelectric capacitors having one terminal connected to the output nodes respectively and the other terminal commonly receiving the control signal; and

third and fourth ferroelectric capacitors having one terminal connected to the output nodes respectively and the other terminal connected to a ground voltage.

16. The nonvolatile ferroelectric memory device of claim 15, wherein the number of the third and fourth ferroelectric capacitors is increased according to the loading level of the output nodes.

17. The nonvolatile ferroelectric memory device of claim 13, wherein the read control means comprises first and second switch means for selectively connecting the read bitline pairs to ground voltages in response to the control signal and a potential of the output nodes.

18. The nonvolatile ferroelectric memory device of claim 12, wherein the sense amplifier comprises:

a pull-up driving means for selectively applying a power supply voltage to the read bitlines pairs according to the voltage difference of the read bitline

pairs; and

a latch means storing data loaded on the read bitline for a predetermined time.

19. The nonvolatile ferroelectric memory device of claim 18, wherein the pull-up driving means comprises:

a detecting means for detecting the voltage difference of the read bitline pairs; and

first and second pull-up means for applying a power supply voltage to the read bitline pairs respectively in response to an output signal from the detecting means.

20. The nonvolatile ferroelectric memory device of claim 1, wherein the ferroelectric memory cell array comprises:

a plurality of write bitline pairs;

a plurality of read bitline pairs;

a plurality of common pull-up lines;

a plurality of common pull-down lines;

a plurality of pull-up means for selectively applying a power supply voltage to the plurality of common pull-up lines respectively in response to the control signal;

a plurality of pull-down means for selectively connecting the plurality of common pull-down lines to

ground voltages respectively in response to the control signal;

a plurality of second multi port memory cells connected in column direction between one of the plurality of write bitline pairs and one of the plurality of read bitline pairs;

a write driving means connected between one of the plurality of write bitline pairs; and

a sense amplifier connected between one of the plurality of read bitline pairs.

21. The nonvolatile ferroelectric memory device of claim 20, wherein the second multi port memory cell comprises:

a first latch means for amplifying a high level by using the voltage difference between output nodes;

a plurality of write control means for selectively connecting the bitlines with output nodes in response to the control signal;

a storage means including a plurality of ferroelectric capacitors;

a second latch means for amplifying a low level by using the voltage difference between output nodes; and

a plurality of read control means for changing a voltage level of the read bitline pair in response to the control signal and a potential of the output nodes.

22. The nonvolatile ferroelectric memory device of claim 21, wherein the latch means comprises PMOS transistors cross-coupled between the output nodes.

23. The nonvolatile ferroelectric memory device of claim 21, wherein the storage means comprises:

first and second ferroelectric capacitors having one terminal connected to the output nodes respectively and the other terminal commonly receiving the control signal; and

third and fourth ferroelectric capacitors having one terminal connected to the output nodes respectively and the other terminal connected to a ground voltage.

24. The nonvolatile ferroelectric memory device of claim 22, wherein the number of the third and fourth ferroelectric capacitors increases according to the loading level of the output nodes.

25. The nonvolatile ferroelectric memory device of claim 20, wherein the sense amplifier comprises:

a pull-up driving means for selectively applying a power supply voltage to the read bitlin pairs according to the voltage difference of the read bitline pairs; and

a latch means for storing data loaded on the read bitlines for a predetermined time.

26. The nonvolatile ferroelectric memory device of claim 25, wherein the pull-up driving means comprises:

a detecting means for detecting the voltage difference of the read bitline pairs; and

first and second pull-up means for applying a power supply voltage to the read bitline pairs respectively in response to an output signal from the detecting means.